a plurality of data wirings formed on the substrate substantially orthogonal to the gate wirings;

a plurality of pixel electrodes formed in a plurality of pixel areas decided by the gate wirings and the data wirings and arranged in a matrix shape;

A thin film transistor formed in each of the pixel areas and structured planar type having an operating semiconductor layer formed on the substrate, a gate insulating film formed on the operating semiconductor layer, a gate electrode formed on the gate insulating film and connected to one of the gate wirings, first and second semiconductor layers formed on both sides of the operating semiconductor layer including impurity, a source electrode including the first semiconductor layer electrically connected to the pixel electrode via a contact window opened to first and second insulating layers laminated on the first semiconductor layer, and a drain electrode including the second semiconductor layer and connected to the data wirings; and

a plurality of storage capacitor electrodes using the first semiconductor layer as a first storage capacitor electrode, having a second storage capacitor electrode being formed between the first insulating film and the second insulating film and connected to a storage capacitor wiring maintained at a predetermined potential, wherein at least a first storage capacitor is structured by the first storage capacitor electrode, the first insulating film and the second storage capacitor electrode, and a second storage capacitor is structured by the second storage capacitor electrode, the second insulating film and the pixel electrode.